Refine Search

Search Results -

Terms	Documents
(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell)	12

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, January 04, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell)	12	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell)	3

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, January 04, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell)	3	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell)	12	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(439/68 |716/16 |716/17 |710/100 |710/300 |710/8 |710/72 |710/305 |712/11 |712/14 |712/18 |326/38 |326/39 |326/41).ccls.	9135

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, January 04, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	710/100,300,8,72,305;712/11,14,18;716/16,17;326/38,39,41;439/68.ccls.	9135	L3
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell)	3	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell)	12	L1

END OF SEARCH HISTORY

Results for "((programmable cell)<in>metadata) and bus"

e-mail printer friendly

Your search matched 3 of 1293212 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

View Session History

New Search

Modify Search

((programmable cell)<in>metadata) and bus

Check to search only within this results set

» Key

Display Format: Citation Citation & Abstract

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1. **Data-driven array processor for video signal processing**
Schmidt, U.; Caesar, K.; Himmel, T.;
Consumer Electronics, IEEE Transactions on
Volume 36, Issue 3, Aug 1990 Page(s):327 - 333
Digital Object Identifier 10.1109/30.103139
AbstractPlus | Full Text: PDF(616 KB) IEEE JNL

2. **Programmable logic machine (A programmable cell array)**
Skokan, Z.E.;
Solid-State Circuits, IEEE Journal of
Volume 18, Issue 5, Oct 1983 Page(s):572 - 578
AbstractPlus | Full Text: PDF(1176 KB) IEEE JNL

3. **Low power mixed signal microprocessor for programmable cell powered urinary incontinence stimulator**
Mouine, J.;
Electronics Letters
Volume 36, Issue 23, 9 Nov. 2000 Page(s):1913 - 1915
Digital Object Identifier 10.1049/el:20001346
AbstractPlus | Full Text: PDF(332 KB) IEE JNL

Programmable logic machine (A programmable cell array)

Skokan, Z.E.

This paper appears in: **Solid-State Circuits, IEEE Journal of**
Publication Date: Oct 1983
Volume: 18 , Issue: 5
On page(s): 572 - 578
ISSN: 0018-9200
Posted online: 2003-01-06 16:59:38.0

Abstract
The PLM is a single mask, **programmable cell** array with complete interconnect. It is 100% wireable and 100% testable with built-in LSSD, it achieves subnanosecond cell delay and 400-gate complexity with less than 1 W of power, and it is fabricated through a low-density process resulting in low cost and a four-day turnaround. This paper describes why the PLM was developed, its operational characteristics, and how it differs from conventional gate arrays.

Index Terms
Inspec
Controlled Indexing
Not Available

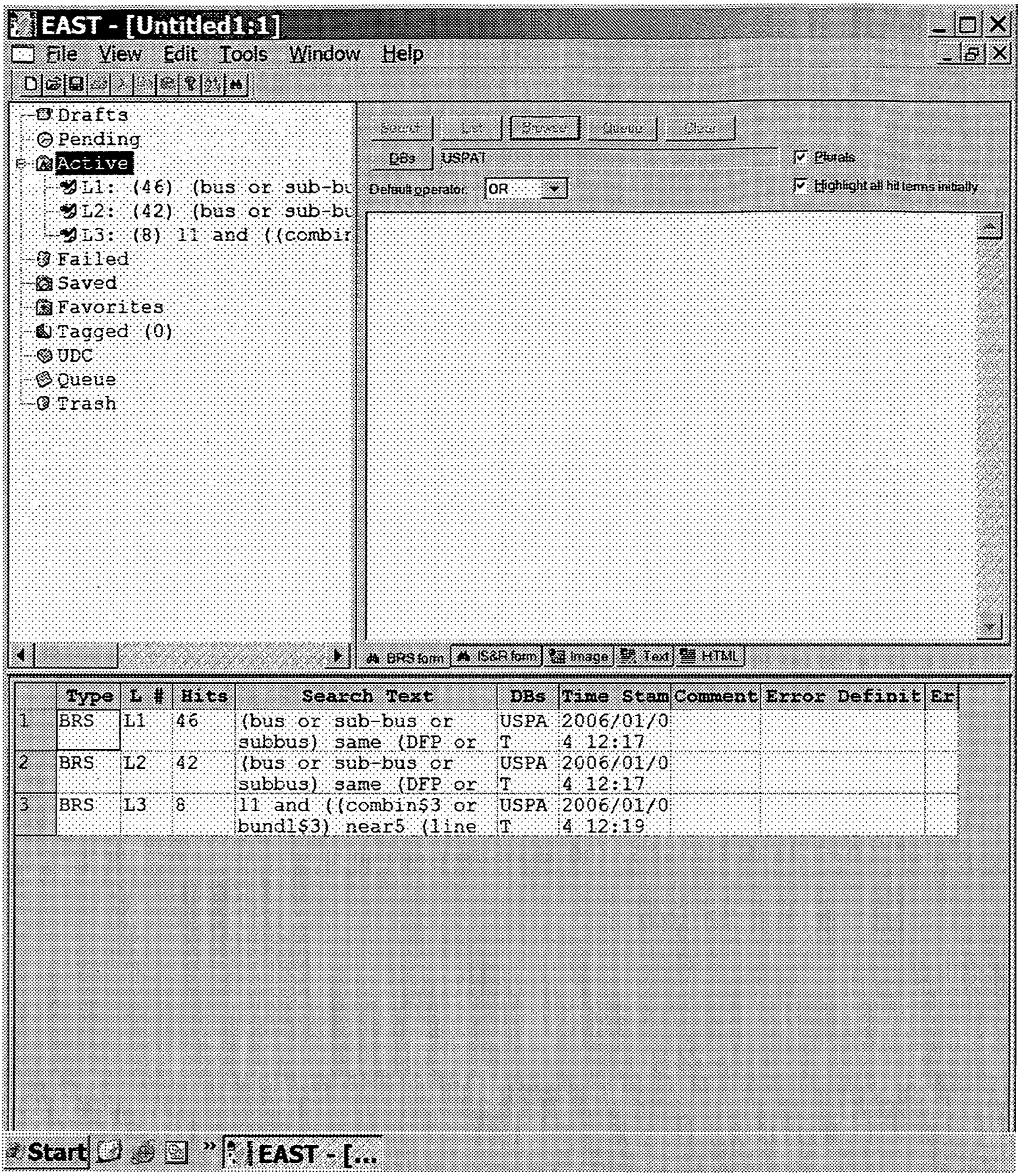
Non-controlled Indexing
Bipolar integrated circuits Cellular arrays Integrated circuit technology Integrated logic circuits Large scale integration bipolar integrated circuits cellular arrays integrated circuit technology integrated logic circuits large scale integration
Author Keywords
Not Available

References

No references available on IEEE Xplore.

Citing Documents

No citing documents available on IEEE Xplore.


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (46) (bus or sub-bu
L2: (42) (bus or sub-bu
L3: (8) l1 and ((combir
Failed
Saved
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Tagged (0)
UDC
Queue
Trash
Search
List
Browse
Queue
Clear
DBs
USPAT
Plurals
Highlight all hit terms initially
Default operator:
OR
BRS form
IS&R form
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Type L # Hits Search Text DBs Time Stam Comment Error Definit Er
1 BRS L1 46 (bus or sub-bus or subbus) same (DFP or USPAT 2006/01/04 12:17
2 BRS L2 42 (bus or sub-bus or subbus) same (DFP or USPAT 2006/01/04 12:17
3 BRS L3 8 l1 and ((combin$3 or bundl$3) near5 (line USPAT 2006/01/04 12:19
Start
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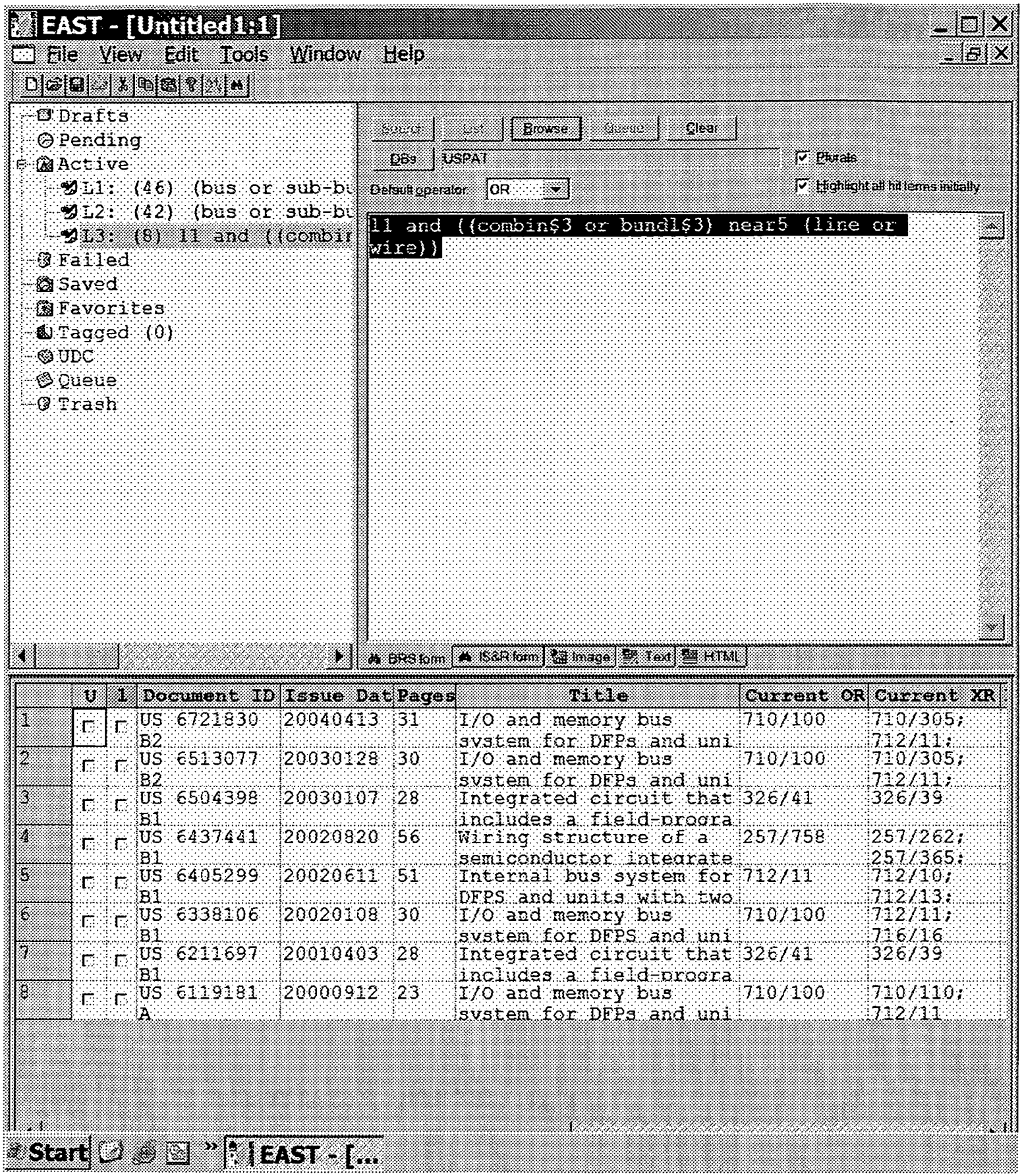

	U	I	Document ID	Issue Dat	Pages	Title	Current OR	Current XR
1	☐	☐	US 6721830 B2	20040413	31	I/O and memory bus system for DFPs and uni	710/100	710/305; 712/11;
2	☐	☐	US 6513077 B2	20030128	30	I/O and memory bus system for DFPs and uni	710/100	710/305; 712/11;
3	☐	☐	US 6504398 B1	20030107	28	Integrated circuit that includes a field-progra	326/41	326/39
4	☐	☐	US 6437441 B1	20020820	56	Wiring structure of a semiconductor integrate	257/758	257/262; 257/365;
5	☐	☐	US 6405299 B1	20020611	51	Internal bus system for DFPS and units with two	712/11	712/10; 712/13;
6	☐	☐	US 6338106 B1	20020108	30	I/O and memory bus system for DFPS and uni	710/100	712/11; 716/16
7	☐	☐	US 6211697 B1	20010403	28	Integrated circuit that includes a field-progra	326/41	326/39
8	☐	☐	US 6119181 A	20000912	23	I/O and memory bus system for DFPs and uni	710/100	710/110; 712/11